**Tutorial 5**

Q1

1. 128 byte 1-way cache with 16 bytes per line (direct mapped) L = 16 K = 1 N = 8

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Hexadecimal | Binary | Offset | Set | Tag | Hit or Miss |
| 0000 | 0000 0000 0000 0000 | 0000 | 000 | 0000 0000 0 | Miss |
| 0004 | 0000 0000 0000 0004 | 0004 | 000 | 0000 0000 0 | Hit |
| 000C | 0000 0000 0000 1100 | 1100 | 000 | 0000 0000 0 | Hit |
| 00D0 | 0000 0000 1101 0000 | 0000 | 101 | 0000 0000 1 | Miss |
| 00E0 | 0000 0000 1110 0000 | 0000 | 110 | 0000 0000 1 | Miss |
| 1130 | 0001 0001 0011 0000 | 0000 | 011 | 0001 0001 0 | Miss |
| 0028 | 0000 0000 0010 1000 | 1000 | 010 | 0000 0000 0 | Miss |
| 113C | 0001 0001 0011 1100 | 1100 | 011 | 0001 0001 0 | Hit |
| 2204 | 0010 0010 0000 0100 | 0100 | 000 | 0010 0010 0 | Miss |
| 0010 | 0000 0000 0001 0000 | 0000 | 001 | 0000 0000 0 | Miss |
| 0004 | 0000 0000 0000 0100 | 0100 | 000 | 0000 0000 0 | Miss |
| 0040 | 0000 0000 0100 0000 | 0000 | 100 | 0000 0000 0 | Miss |
| 2208 | 0010 0010 0000 1000 | 1000 | 000 | 0010 0010 0 | Miss |
| 0008 | 0000 0000 0000 1000 | 1000 | 000 | 0000 0000 0 | Miss |
| 00A0 | 0000 0000 1010 0000 | 0000 | 010 | 0000 0000 1 | Miss |
| 0004 | 0000 0000 0000 0100 | 0100 | 000 | 0000 0000 0 | Hit |
| 1104 | 0001 0001 0000 0100 | 0100 | 000 | 0001 0001 0 | Miss |
| 000C | 0000 0000 0000 1100 | 1100 | 000 | 0000 0000 0 | Miss |
| 0084 | 0000 0000 1000 0100 | 0100 | 000 | 0000 0000 1 | Miss |
| 000C | 0000 0000 0000 1100 | 1100 | 000 | 0000 0000 0 | Miss |
| 3390 | 0011 0011 1001 0000 | 0000 | 001 | 0011 0011 1 | Miss |
| 00B0 | 0000 0000 1011 0000 | 0000 | 011 | 0000 0000 1 | Miss |
| 1100 | 0001 0001 0000 0000 | 0000 | 000 | 0001 0001 0 | Miss |
| 0028 | 0000 0000 0010 1000 | 1000 | 010 | 0000 0000 0 | Miss |
| 0070 | 0000 0000 0111 0000 | 0000 | 111 | 0000 0000 0 | Miss |
| 00D0 | 0000 0000 1101 0000 | 0000 | 101 | 0000 0000 1 | Hit |
| 0008 | 0000 0000 0000 1000 | 1000 | 000 | 0000 0000 0 | Miss |
| 3394 | 0011 0011 1001 0100 | 0100 | 001 | 0011 0011 1 | Hit |

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1. 128 byte 2-way set associative cache with 16 bytes per line L = 16 K = 2 N = 4

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| hex | binary | offset | set | tag | Hit or Miss |
| 0000 | 0000 0000 0000 0000 | 0000 | 00 | 0000 0000 00 | Miss |
| 0004 | 0000 0000 0000 0004 | 0004 | 00 | 0000 0000 00 | Hit |
| 000C | 0000 0000 0000 1100 | 1100 | 00 | 0000 0000 00 | Hit |
| 00D0 | 0000 0000 1101 0000 | 0000 | 01 | 0000 0000 11 | Miss |
| 00E0 | 0000 0000 1110 0000 | 0000 | 10 | 0000 0000 10 | Miss |
| 1130 | 0001 0001 0011 0000 | 0000 | 11 | 0001 0001 00 | Miss |
| 0028 | 0000 0000 0010 1000 | 1000 | 10 | 0000 0000 00 | Miss |
| 113C | 0001 0001 0011 1100 | 1100 | 11 | 0001 0001 00 | Hit |
| 2204 | 0010 0010 0000 0100 | 0100 | 00 | 0010 0010 00 | Miss |
| 0010 | 0000 0000 0001 0000 | 0000 | 01 | 0000 0000 00 | Miss |
| 0004 | 0000 0000 0000 0100 | 0100 | 00 | 0000 0000 00 | Hit |
| 0040 | 0000 0000 0100 0000 | 0000 | 00 | 0000 0000 01 | Miss |
| 2208 | 0010 0010 0000 1000 | 1000 | 00 | 0010 0010 00 | Miss |
| 0008 | 0000 0000 0000 1000 | 1000 | 00 | 0000 0000 00 | Miss |
| 00A0 | 0000 0000 1010 0000 | 0000 | 10 | 0000 0000 10 | Miss |
| 0004 | 0000 0000 0000 0100 | 0100 | 00 | 0000 0000 00 | Hit |
| 1104 | 0001 0001 0000 0100 | 0100 | 00 | 0001 0001 00 | Miss |
| 000C | 0000 0000 0000 1100 | 1100 | 00 | 0000 0000 00 | Hit |
| 0084 | 0000 0000 1000 0100 | 0100 | 00 | 0000 0000 10 | Miss |
| 000C | 0000 0000 0000 1100 | 1100 | 00 | 0000 0000 00 | Hit |
| 3390 | 0011 0011 1001 0000 | 0000 | 01 | 0011 0011 10 | Miss |
| 00B0 | 0000 0000 1011 0000 | 0000 | 11 | 0000 0000 10 | Miss |
| 1100 | 0001 0001 0000 0000 | 0000 | 00 | 0001 0001 00 | Miss |
| 0028 | 0000 0000 0010 1000 | 1000 | 10 | 0000 0000 00 | Hit |
| 0070 | 0000 0000 0111 0000 | 0000 | 11 | 0000 0000 01 | Miss |
| 00D0 | 0000 0000 1101 0000 | 0000 | 01 | 0000 0000 11 | Miss |
| 0008 | 0000 0000 0000 1000 | 1000 | 00 | 0000 0000 00 | Hit |
| 3394 | 0011 0011 1001 0100 | 0100 | 01 | 0011 0011 10 | Hit |

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1. 128 byte 4-way set associative cache with 16 bytes per line L = 16 K = 4 N = 2

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| hex | binary | offset | set | tag | Hit or Miss |
| 0000 | 0000 0000 0000 0000 | 0000 | 0 | 0000 0000 000 | Miss |
| 0004 | 0000 0000 0000 0004 | 0004 | 0 | 0000 0000 000 | Hit |
| 000C | 0000 0000 0000 1100 | 1100 | 0 | 0000 0000 000 | Hit |
| 00D0 | 0000 0000 1101 0000 | 0000 | 1 | 0000 0000 110 | Miss |
| 00E0 | 0000 0000 1110 0000 | 0000 | 0 | 0000 0000 111 | Miss |
| 1130 | 0001 0001 0011 0000 | 0000 | 1 | 0001 0001 001 | Miss |
| 0028 | 0000 0000 0010 1000 | 1000 | 0 | 0000 0000 001 | Miss |
| 113C | 0001 0001 0011 1100 | 1100 | 1 | 0001 0001 001 | Hit |
| 2204 | 0010 0010 0000 0100 | 0100 | 0 | 0010 0010 000 | Miss |
| 0010 | 0000 0000 0001 0000 | 0000 | 1 | 0000 0000 000 | Miss |
| 0004 | 0000 0000 0000 0100 | 0100 | 0 | 0000 0000 000 | Hit |
| 0040 | 0000 0000 0100 0000 | 0000 | 0 | 0000 0000 010 | Miss |
| 2208 | 0010 0010 0000 1000 | 1000 | 0 | 0010 0010 000 | Hit |
| 0008 | 0000 0000 0000 1000 | 1000 | 0 | 0000 0000 000 | Hit |
| 00A0 | 0000 0000 1010 0000 | 0000 | 0 | 0000 0000 101 | Miss |
| 0004 | 0000 0000 0000 0100 | 0100 | 0 | 0000 0000 000 | Hit |
| 1104 | 0001 0001 0000 0100 | 0100 | 0 | 0001 0001 000 | Miss |
| 000C | 0000 0000 0000 1100 | 1100 | 0 | 0000 0000 000 | Hit |
| 0084 | 0000 0000 1000 0100 | 0100 | 0 | 0000 0000 100 | Miss |
| 000C | 0000 0000 0000 1100 | 1100 | 0 | 0000 0000 000 | Hit |
| 3390 | 0011 0011 1001 0000 | 0000 | 1 | 0011 0011 100 | Miss |
| 00B0 | 0000 0000 1011 0000 | 0000 | 1 | 0000 0000 101 | Miss |
| 1100 | 0001 0001 0000 0000 | 0000 | 0 | 0001 0001 000 | Hit |
| 0028 | 0000 0000 0010 1000 | 1000 | 0 | 0000 0000 001 | Miss |
| 0070 | 0000 0000 0111 0000 | 0000 | 1 | 0000 0000 011 | Miss |
| 00D0 | 0000 0000 1101 0000 | 0000 | 1 | 0000 0000 110 | Miss |
| 0008 | 0000 0000 0000 1000 | 1000 | 0 | 0000 0000 000 | Hit |
| 3394 | 0011 0011 1001 0100 | 0100 | 1 | 0011 0011 100 | Hit |

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1. 128 byte 8-way associative cache with 16 bytes per line L = 16 K = 8 N = 1

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| hex | binary | offset | set | tag | Hit or Miss |
| 0000 | 0000 0000 0000 0000 | 0000 | Null | 0000 0000 0000 | Miss |
| 0004 | 0000 0000 0000 0004 | 0004 | Null | 0000 0000 0000 | Hit |
| 000C | 0000 0000 0000 1100 | 1100 | Null | 0000 0000 0000 | Hit |
| 00D0 | 0000 0000 1101 0000 | 0000 | Null | 0000 0000 1101 | Miss |
| 00E0 | 0000 0000 1110 0000 | 0000 | Null | 0000 0000 1110 | Miss |
| 1130 | 0001 0001 0011 0000 | 0000 | Null | 0001 0001 0011 | Miss |
| 0028 | 0000 0000 0010 1000 | 1000 | Null | 0000 0000 0010 | Miss |
| 113C | 0001 0001 0011 1100 | 1100 | Null | 0001 0001 0011 | Hit |
| 2204 | 0010 0010 0000 0100 | 0100 | Null | 0010 0010 0000 | Miss |
| 0010 | 0000 0000 0001 0000 | 0000 | Null | 0000 0000 0001 | Miss |
| 0004 | 0000 0000 0000 0100 | 0100 | Null | 0000 0000 0000 | Hit |
| 0040 | 0000 0000 0100 0000 | 0000 | Null | 0000 0000 0100 | Miss |
| 2208 | 0010 0010 0000 1000 | 1000 | Null | 0010 0010 0000 | Hit |
| 0008 | 0000 0000 0000 1000 | 1000 | Null | 0000 0000 0000 | Hit |
| 00A0 | 0000 0000 1010 0000 | 0000 | Null | 0000 0000 1010 | Miss |
| 0004 | 0000 0000 0000 0100 | 0100 | Null | 0000 0000 0000 | Hit |
| 1104 | 0001 0001 0000 0100 | 0100 | Null | 0001 0001 0000 | Miss |
| 000C | 0000 0000 0000 1100 | 1100 | Null | 0000 0000 0000 | Hit |
| 0084 | 0000 0000 1000 0100 | 0100 | Null | 0000 0000 1000 | Miss |
| 000C | 0000 0000 0000 1100 | 1100 | Null | 0000 0000 0000 | Hit |
| 3390 | 0011 0011 1001 0000 | 0000 | Null | 0011 0011 1001 | Miss |
| 00B0 | 0000 0000 1011 0000 | 0000 | Null | 0000 0000 1011 | Miss |
| 1100 | 0001 0001 0000 0000 | 0000 | Null | 0001 0001 0000 | Hit |
| 0028 | 0000 0000 0010 1000 | 1000 | Null | 0000 0000 0010 | Miss |
| 0070 | 0000 0000 0111 0000 | 0000 | Null | 0000 0000 0111 | Miss |
| 00D0 | 0000 0000 1101 0000 | 0000 | Null | 0000 0000 1101 | Miss |
| 0008 | 0000 0000 0000 1000 | 1000 | Null | 0000 0000 0000 | Hit |
| 3394 | 0011 0011 1001 0100 | 0100 | Null | 0011 0011 1001 | Hit |

12 hits out of 28

Q2).

Instruction Miss Rate = 2%

Data Miss Rate = 4%

CPI = 2

Miss Penalty = 100

Load/Store Instructions = 36%

Instruction Miss Cycles = (I) x (Instruction Miss Rate) x (Miss Penalty)

= I x 0.02 x 100

= 2(I)

Data Miss Cycles = (I) x (Load/Store Instructions) x (Data Miss Rate) x (Miss Penalty)

= I x 0.36 x 0.04 x 100

= 1.44(I)

Total Memory Stalls = (Instruction Miss Cycles) + (Data Miss Cycles)

= 2(I) + 1.44(I)

= 3.44(I)

CPI stall = (CPI) + (Total Memory Stalls)

= 2 + 3.44

= 5.44

To determine how much faster we will divide the CPU time with stalls by the CPU time with a perfect cache.

(CPU time with stalls / CPU time with perfect cache)

=

((I) x (CPI stall) x (Clock Cycle) / (I) x (CPI perfect) x (Clock Cycle))

(I) and (Clock Cycle) cancel out leaving:

(CPI Stall / CPI Perfect)

= (5.44 / 2)

= 2.72

A CPU with a perfect CPU is 2.72 times faster.

Q3).

Part 1)

There is 64 bytes, it will access them in words, i.e. every 4 bytes, meaning there is 16 words in total.

To reach the first word will take 50 ns and for the remaining 15 word will take 5 ns.

Noting that the access time is 2.5 ns we can make the following formula.

t main = (2.5) + (50) + (5)(15) + (2.5)

= 130 ns

Part 2)

We will be using the formula:

T eff = h(t cache) + (1-h)(t main)

for this question primarily, first with H = 0.95 and again with H = 0.97 with the new t main value.

**H = 0.95**

t eff = (0.95)(2.5) + (1 – 0.95)(130)

= 8.875 ns

**H = 0.97**

First we must calculate the new t main as we are now working with 128 bytes.

It is 128 bytes, i.e. 32 words. We will use the same formula as in part 1 but replacing the appropriate value.

t main = (2.5) + (50) + (5)(31) + (2.5)

= 210 ns

Now that we have done that we may find the new t eff

t eff = (0.97)(2.5) + (1 – 0.97)(210)

= 8.725 ns

From the above results we can conclude that the average memory address time is reduced.

Q4).

1.

From the question we are able to get the following values.

Cache line size = 1

Clock Cycle = 1

Clock Cycle to access 32 bit word = 4

Formula for the miss penalty is:

Miss Penalty = Cache line size x (Clock Cycle to access 32 bit word + Clock Cycle)

= 1 x (4 + 1)

= 5

From this we can conclude the miss penalty for when the cache line size is one word is 5 clock cycles.

2.

Cache line size = 4

Clock Cycle = 1

Clock Cycle to access 32 bit word = 4

Using the same formula as before we get:

Miss Penalty = Cache line size x (Clock Cycle to access 32 bit word + Clock Cycle)

= 4 x (4 + 1)

= 20

The miss penalty we can conclude is 20 clock cycles for 4 words with non-burst transfer.

3.

We are working with 4 words and every clock cycle after the first being 1 clock cycle and from the first part we know that the penalty for the first word is 5 clock cycles, we can conclude that the miss penalty would be:

Miss Penalty

=

Miss Penalty of first word + ((Number of Words – 1) x Miss penalty for subsequent Words)

= 5 + ((4 – 1) x 1)

= 8

The Miss penalty 4 words where transfer is executed at 1 clock cycle per word transfer is 8 clock cycles.